IN THE SPECIFICATION:

Please amend paragraph number **[0005]** as follows:

**[0005]** One solution which is capable of providing the necessary number of capacitors on a DRAM memory device is the formation of stacked-type or trench-type capacitor cells having larger surface areas. Typical manners which may be used for increasing capacitor cell surface area for stacked-type capacitor cells are to use either fin-type capacitor cells, pillar-type capacitor cells, striated capacitor cell walls, rippled capacitor cell walls, or ~~roughened-surface-type~~ roughened-surface-type capacitor cell walls. Such types of stacked capacitor cells are described in United States Patents 5,061,650, 5,240,871, 5,300,801, 5,466,627, 5,519,238, 5,623,243, 5,637,523, 5,656,536, 5,827,783, 5,843,822, and 5,879,987. It is further known to selectively texturize polysilicon electrodes with respect to neighboring dielectric surfaces in DRAM memory devices, such as described in United States Patent 5,830,793.

Please amend paragraph number **[0008]** as follows:

**[0008]** The present invention comprises a method of forming a rippled or corrugated capacitor cell wall having increased surface area used in capacitors in DRAM memory chips and semiconductor devices. More specifically, the invention relates to a method of forming a rippled or corrugated capacitor cell wall having increased surface area in a DRAM memory device using alternating layers of silicate glass which are subsequently etched to form the corrugated cell wall structure. The corrugated capacitor cell is constructed of alternating layers of germanium ~~boro-phospho~~ boro-phospho silicate glass (Ge-BPSG) and boro-phospho silicate glass (BPSG) or nitro silicate glass (NSG) and etched to form the rippled or corrugated cell wall. The formation of corrugated wall capacitor cells using the methods disclosed herein may be accomplished using current semiconductor device process technologies for materials having deposition rates comparable to those of the materials normally used for deposition in such process technologies.

Please amend paragraph number **[0016]** as follows:

**[0016]** FIG. 5 illustrates a cross-sectional side view of the formation of an ~~etch-resistant~~ etch-resistant layer over the alternating first layers and second layers of doped silicate glass prior to etching.

Please amend paragraph number **[0020]** as follows:

**[0020]** Deposition of a second layer 120 of doped silicon glass, typically Ge-BPSG, over the first layer 110 is illustrated in drawing FIG. 3. As with the first layer 110, the second layer 120 is deposited using CVD and PECVD techniques. Alternate layering of first layers 110 and second layers 120 forms a capacitor cell having a desired thickness. Deposition of the alternating layers occurs in a cluster formation, in either atmospheric or subatmospheric conditions in a reaction chamber known in the art. Deposition of the first layer 110 and second layer 120 thereby forms individual capacitance units which ultimately result in individual corrugated capacitor cells 100 of ~~substrate10~~ substrate 10 as depicted in drawing FIG. 4.

Please amend paragraph number **[0024]** as follows:

**[0024]** Referring to drawing FIG. 1A, after the corrugated capacitor cells 100 are formed having corrugated or rippled side wall surface 115, a dielectric layer 116 is deposited over the side wall surface 115 and the upper etch-resistant layer 130. The dielectric material may be $Si_3N_4$, $Ta_2O_5$, BST, etc. After the dielectric layer 116 is deposited, an anneal process is performed on the substrate 10 used to form the semiconductor die for the redistribution of dopants used therein. Subsequently, a top electrode layer 118 is deposited over the dielectric layer 116 to form the top electrode for each corrugated capacitor cell 100. The material used for the layer 118 forming the top electrode of the corrugated capacitor cell 100 may be Si-Ge.